REMARKS

By the foregoing amendments a correction has been made on page 14 in the specification and claims 14, 15, 17, 22, 23, and 25 have been amended. Thus, claims 1-29 remain in the application. Claims 1-13 stand allowed.

Claims 17-19 and 25-27 were objected to the outstanding Office Action as being dependent upon a rejected base claim, but it was stated that these claims would be allowable if rewritten in independent form to include the limitations of the base claim and any intervening claims. Responsive to this objection and indication of allowable subject matter, by the above amendments claims 17 and 25 have been rewritten in independent form to include the limitations of the claims from which they previously depended. Accordingly, it is respectfully submitted that claims 17-19 and 25-27 are in condition for allowance and such action by the Examiner is respectfully requested.

The objection to the disclosure because of the informality on page 14, line 8, has been corrected by the above amendments in the manner suggested in the Office Action. Reconsideration and withdrawal of the objection to the disclosure is respectfully requested.

Claims 14-16, 21-24 and 29 were rejected in the Office Action under 35 U.S.C. §103(a) as being unpatentable over the patent to Dauksher et al., U.S. Patent No. 6,320,754, and Jimarez et al., U.S. Patent No. 6,191,952. The references were cited for the reasons and in the manner stated on pages 2-10 of the Office Action.

Claims 20 and 28 have been rejected in the Office Action under 35 U.S.C. §103(a) as being unpatentable over Dauksher et al. and Jimarez et al. in view of the patent to Bernier et al., U.S. Patent Application Publication No. 2002/0195707. The cited references were relied upon as set forth on pages 10 and 11 of the Office Action.

These rejections of the application claims are hereby traversed and reconsideration thereof is respectfully requested in view of the above amendments to the claims and Applicants remarks set forth below.

The primary reference to Dauksher et al. relied upon in the aforementioned rejections of the application claims discloses an apparatus for the reduction of interfacial stress caused by differential thermal expansion in an integrated circuit package. A solution to interfacial stress caused by differential thermal expansion in an integrated circuit package proposed by Dauksher et al. involves the use of an annular ring which surrounds the integrated circuit or the substrate carrying the integrated circuit which is soldered to a PC board or substrate. The annular ring has a larger coefficient of thermal expansion than the integrated circuit or substrate which it surrounds. The annular ring is dimensioned so that when placed around the integrated circuit or substrate at an elevated temperature, when cooled it causes the integrated circuit or substrate to contract more than it would without the ring attached. The increased contraction caused in the integrated circuit or substrate by the ring more closely matches the change in length, e.g. contraction, of the PC board that it is attached to by soldered connections. The patentees state that because the integrated circuit or substrate length change with the ring attached is closer to the PC board length change there is

less stress in the solder that forms the joints between the integrated circuit or substrate and the PC board, and there is less stress in the PC board. However, there is increased compressive stress in the integrated circuit or substrate at room temperature caused by the compressive force of the annular ring which forcibly contracts the integrated circuit or substrate.

In contrast, a fundamental distinction between the invention of Dauksher et al. and the present invention is that with the present invention elongation mismatch between the adherents is reduced through differential heating, rather than by forcibly contracting the integrated circuit or substrate with an annular ring as in Dauksher et al. At room temperature after soldering, the compressive stress on the chip is reduced, not increased as in Dauksher et al. That is, with the present invention each of the semiconductor chip and substrate, for example, are thermally expanded substantially the same amount in a direction along the surfaces thereof to be joined by soldering. In the preferred embodiment this is accomplished by heating the chip and the substrate to different temperatures as a function of the mismatch of their coefficients of thermal expansion, and thereafter assembling the chip and the substrate in contact with one another for the soldering.

The resulting electronic assembly and semiconductor package of the present invention not only have substantially lower coefficient of thermal expansion difference induced elongated mismatches across the respective soldered joints thereof, but the stresses induced in the electronic assembly/semiconductor package as a result of soldering are also substantially reduced, e.g. less than one-half that expected based upon cooling of the substrate and semiconductor chip from the solder solidification

temperature to room temperature following soldering of the solder joints, see page 12 of the specification, the bottom half of the page wherein it is noted that stresses and warpage as well as the normal force on the bump are reduced to less than one-half that in the package made by the conventional method where the substrate and semiconductor chip are cooled together from the solder solidification temperature to room temperature following soldering of the solder joints. Figure 5 of the application drawings graphically illustrates this improvement.

Thus, the electronic assembly and semiconductor package of the present invention do not have increased compressive stress on the integrated circuit as in Dauksher et al., but rather the stresses on the integrated circuit are less than one-half that expected based upon cooling of the substrate and semiconductor chip from the solder solidification temperature to room temperature following soldering of the solder joints. As noted above, in Dauksher et al., the stresses on the integrated circuit are increased, rather than reduced as a result of the use of the annular ring which compresses the integrated circuit at room temperature as described in the patent. The present invention avoids this disadvantage and also the need for the use of an annular ring in the first instance.

The secondary references to Jimarez et al. and Bernier et al. do not provide for the aforementioned deficiencies of Dauksher et al. By the above amendments independent claims 14 and 22 have been amended to positively recite where at the elongation mismatches and the stresses induced thereby in the electronic assembly/semiconductor package are less than one-half that expected based upon cooling the substrate and semiconductor chip from the

solder solidification temperature to room temperature following soldering of the solder joints. As noted above, this clearly distinguishes over Dauksher et al., alone or taken with Jimarez et al. and Bernier et al., wherein the compressive stress is actually increased on the integrated circuit at room temperature in order to lower that on the adjacent soldered joints and substrate joined to the integrated circuit.

In view of the above amendments and remarks, it is respectfully submitted that claims 14-16, 21-24, 28 and 29 as amended now patentably define over the cited references. Accordingly, reconsideration and allowance of these claims and amended claims 17-19 and 25-27 are respectfully requested.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with markings to show changes made."**

To the extent necessary, Applicants petition for an extension of time under 37 CFR §1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 01-2135 (Case No. 219.40779X00) and please credit any excess fees to such deposit account.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Please amend the specification on page 14, in the single paragraph on the page, to read as follows:

This concludes the description of the example embodiment. Although the present invention has been described with reference to one illustrative embodiment thereof, it should be understood that numerous other modifications and embodiments can be devised by those skilled in the art that will fall within the spirit and scope of the principles of this invention. For example, the thermal expansion before soldering is the same for the chip and substrate in the example embodiment but significant benefit can be obtained if the expansions are not identical but at least substantially the same, e.g., [with] within ± 25% of one another or not differing by more than 2 ppm/°C. More particularly, reasonable variations and modifications are possible in the component parts and/or arrangements of the subject combination arrangement within the scope of the foregoing disclosure, the drawings and the appended claims without departing from the spirit of the invention. In addition to variations and modifications in the component parts and/or arrangements, alternative uses will also be apparent to those skilled in the art.

IN THE CLAIMS:

Please amend the claims as follows:

14. (Amended) An electronic assembly comprising:

a substrate having a first coefficient of thermal expansion;

a semiconductor chip having a second coefficient of thermal expansion which is different than the first coefficient of thermal expansion;

a plurality of soldered joints connecting the semiconductor chip and substrate;

wherein the chip and substrate across the respective soldered joints of the electronic assembly at room temperature have coefficient of thermal expansion difference induced elongation mismatches and stresses induced thereby in the electronic assembly from soldering; and

wherein the magnitude of the elongation mismatches and the stresses induced thereby in the electronic assembly are less than one-half that expected based upon cooling the substrate and semiconductor chip from the solder solidification temperature to room temperature following soldering of the soldered joints.

15. (Amended) The electronic assembly according to claim 14, wherein the elongation mismatches and the stresses induced thereby in the electronic assembly are reflected in the electronic assembly by at least one of post soldering residual stress, residual plastic deformation in the soldered joints, residual plastic deformation in the substrate, and semiconductor chip warpage.

17. (Amended) [The] An electronic assembly [according to claim 14,] comprising:

a substrate having a first coefficient of thermal expansion;

a semiconductor chip having a second coefficient of thermal expansion which is different than the first coefficient of thermal expansion;

a plurality of soldered joints connecting the semiconductor chip and substrate;

wherein the chip and substrate across the respective soldered joints of the electronic assembly at room temperature have coefficient of thermal expansion difference induced elongation mismatches from soldering; and

wherein the magnitude of the elongation mismatches are less than one-half that expected based upon cooling the substrate and semiconductor chip from the solder solidification temperature to room temperature following soldering of the soldered joints; and

wherein the substrate comprises a plurality of standoff elements upstanding from a surface of the substrate, and wherein the soldered joints connect the semiconductor chip to the tops of respective ones of the standoff elements.

22. (Amended) A semiconductor package comprising:

a package substrate having a first coefficient of thermal expansion of at least 15 ppm/°C, the package substrate having a plurality of contact members;

a semiconductor chip having a coefficient of thermal expansion which is at least 2.7 ppm/°C less than the coefficient of thermal expansion of the package substrate, a front side of the chip having a plurality of solder connections thereon, the semiconductor chip being located on the substrate with the solder connections connected to respective ones of the contact

members by soldered joints electrically coupling the semiconductor chip to the package substrate;

wherein the semiconductor chip and package substrate across the respective soldered joints of the semiconductor package at room temperature have coefficient of thermal expansion difference induced elongation mismatches and stresses induced thereby in the semiconductor package from soldering; and

wherein the magnitude of the elongation mismatches and the stresses induced thereby in the semiconductor package are less than one-half that expected based upon cooling the substrate and semiconductor chip from the solder solidification temperature to room temperature following soldering of the soldered joints.

23. (Amended) The semiconductor package according to claim 22, wherein the elongation mismatches and the stresses induced thereby in the semiconductor package are reflected in the semiconductor package by at least one of post soldering residual stress, residual plastic deformation in the soldered joints, residual plastic deformation in the substrate, and semiconductor chip warpage.

25. (Amended) [The] A semiconductor package [according to claim 22,] comprising:

a package substrate having a first coefficient of thermal expansion of at least 15 ppm/°C, the package substrate having a plurality of contact members;

a semiconductor chip having a coefficient of thermal expansion which is at least 2.7 ppm/°C less than the coefficient of thermal expansion of the package substrate, a front side of the chip having a plurality of solder connections thereon, the semiconductor chip being located on the substrate with the solder connections connected to respective ones of the contact members by soldered joints electrically coupling the semiconductor chip to the package substrate;

wherein the semiconductor chip and package substrate across the respective soldered joints of the semiconductor package at room temperature have coefficient of thermal expansion difference induced elongation mismatches from soldering; and

wherein the magnitude of the elongation mismatches are less than one-half that expected based upon cooling the substrate and semiconductor chip from the solder solidification temperature to room temperature following soldering of the soldered joints; and

wherein the contact members comprise a plurality of standoff elements upstanding from a surface of the substrate, and wherein the soldered joints connect the semiconductor chip to the tops of respective ones of the standoff elements.